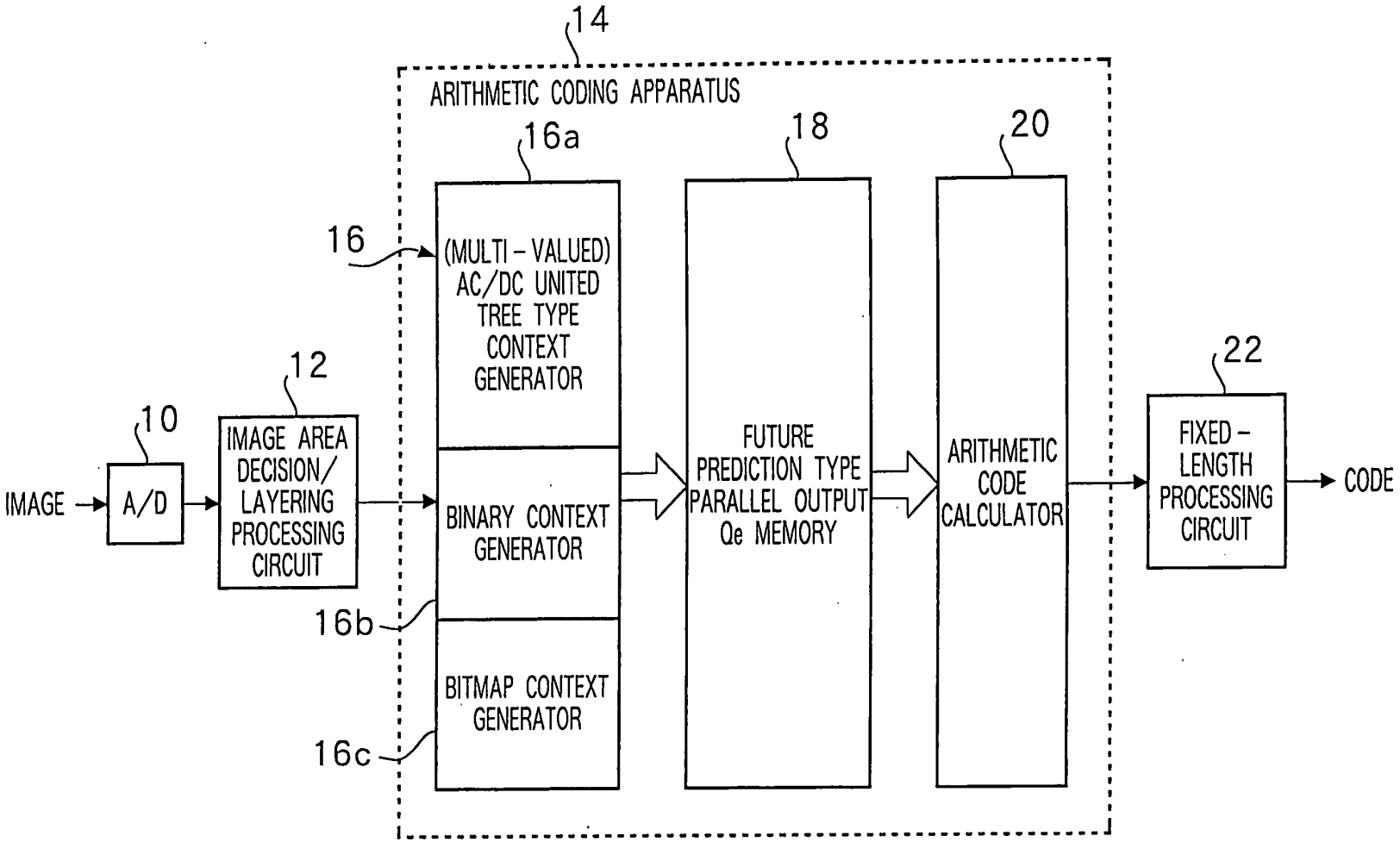

14
ARITHMETIC CODING APPARATUS
16a
18
20
16
(MULTI - VALUED) AC/DC UNITED TREE TYPE CONTEXT GENERATOR
12
22
10
IMAGE
A/D
IMAGE AREA DECISION/ LAYERING PROCESSING CIRCUIT
BINARY CONTEXT GENERATOR
FUTURE PREDICTION TYPE PARALLEL OUTPUT Qe MEMORY
ARITHMETIC CODE CALCULATOR
FIXED - LENGTH PROCESSING CIRCUIT
CODE
16b
BITMAP CONTEXT GENERATOR
16c

FIG. 1

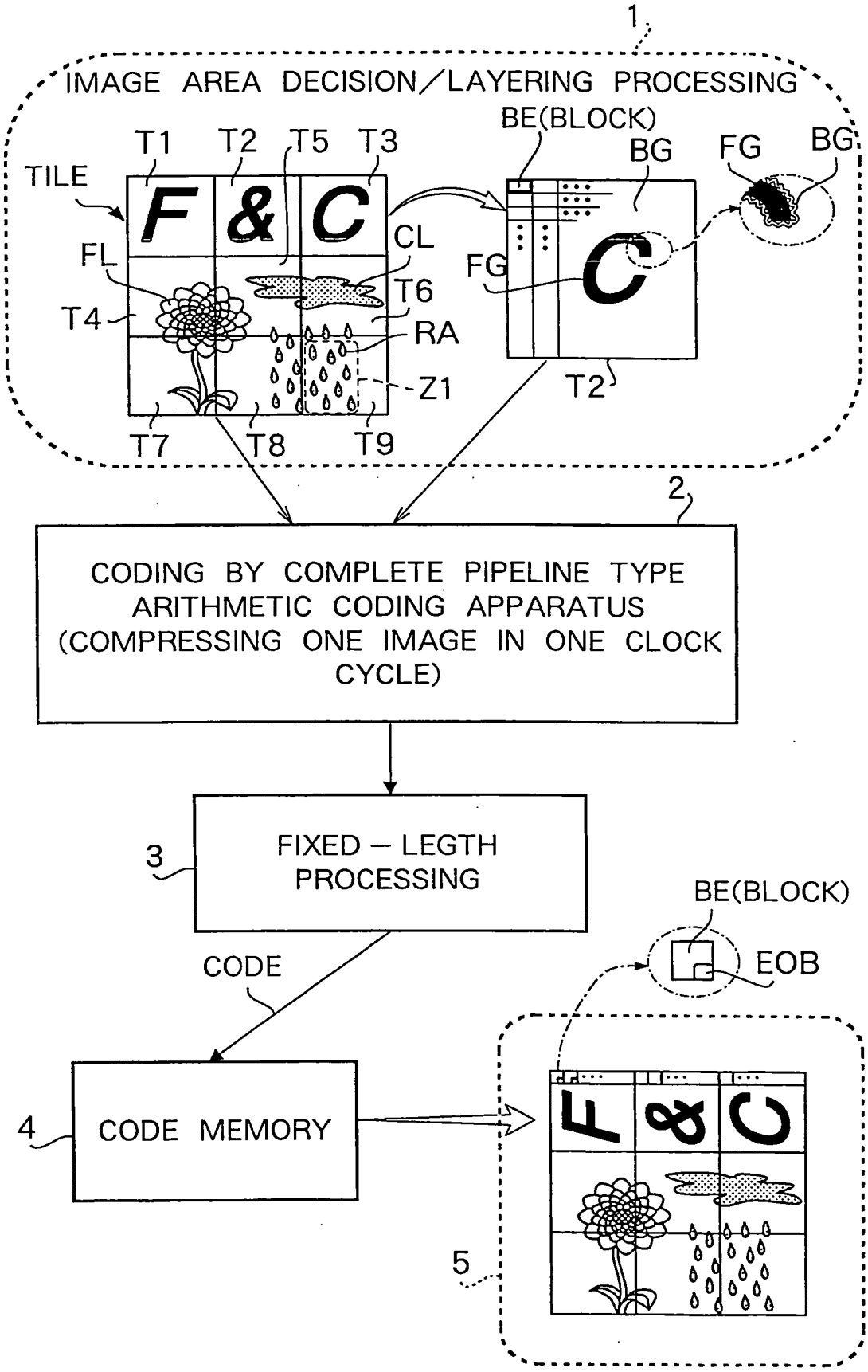

1
IMAGE AREA DECISION/LAYERING PROCESSING
BE(BLOCK)
BG
FG
BG
T1
T2
T5
T3
TILE
F & C
CL
FL
FG
C
T6
T4
RA
Z1
T2
T7
T8
T9
2
CODING BY COMPLETE PIPELINE TYPE ARITHMETIC CODING APPARATUS (COMPRESSING ONE IMAGE IN ONE CLOCK CYCLE)
3
FIXED – LEGTH PROCESSING
BE(BLOCK)
EOB
CODE
4
CODE MEMORY
F & C
5

FIG. 2

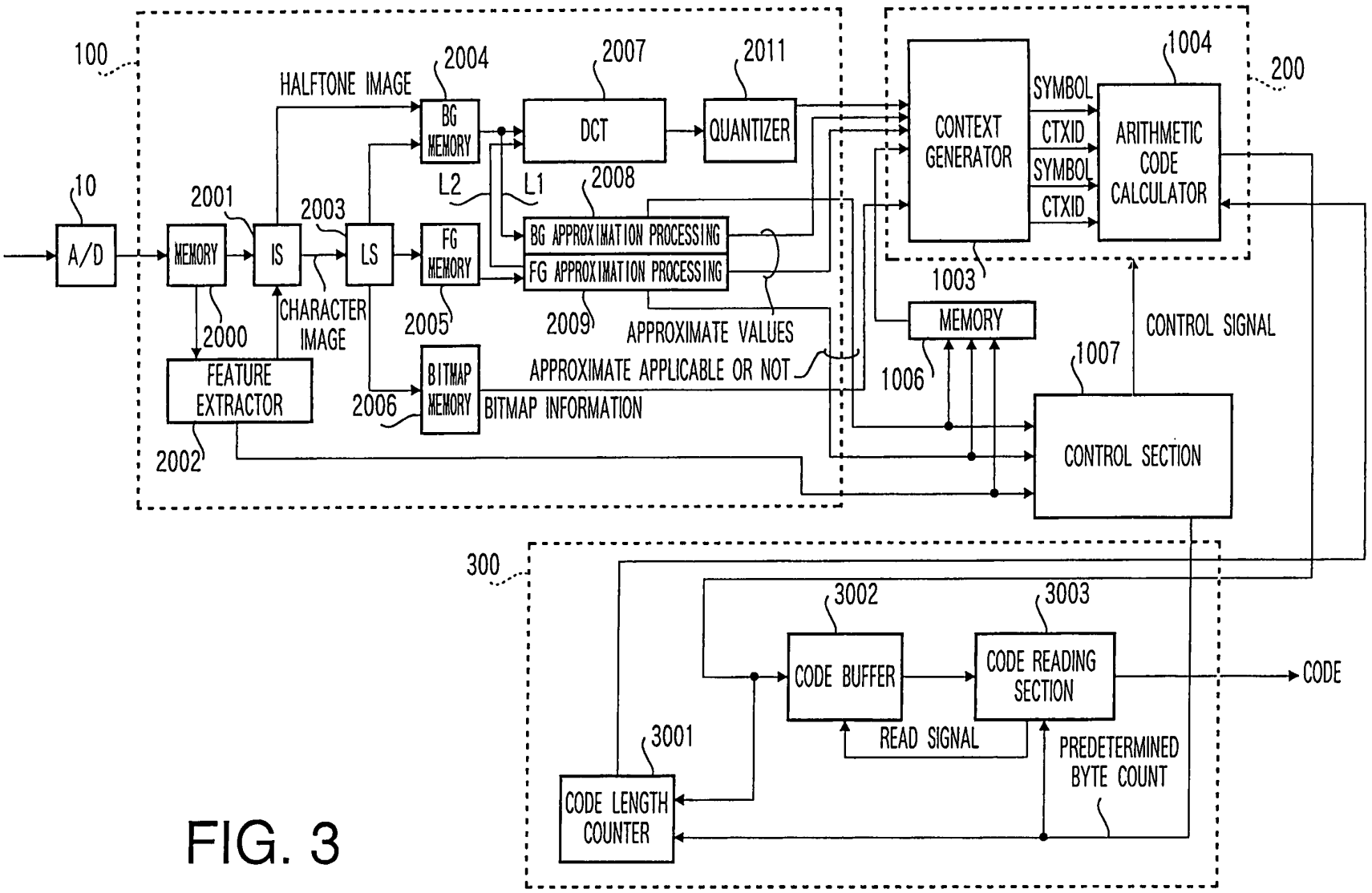

100
10
A/D
2001
MEMORY
2000
FEATURE EXTRACTOR
2002
IS
CHARACTER IMAGE
2003
LS
HALFTONE IMAGE
2004
BG MEMORY
L2
L1
FG MEMORY
2005
2006
BITMAP MEMORY
BITMAP INFORMATION
2007
DCT
2008
BG APPROXIMATION PROCESSING
FG APPROXIMATION PROCESSING
2009
APPROXIMATE VALUES
APPROXIMATE APPLICABLE OR NOT
2011
QUANTIZER
200
CONTEXT GENERATOR
SYMBOL
CTXID
SYMBOL
CTXID
1004
ARITHMETIC CODE CALCULATOR
1003
MEMORY
1006
1007
CONTROL SECTION
CONTROL SIGNAL
300
3002
CODE BUFFER
3003
CODE READING SECTION
CODE
READ SIGNAL
PREDETERMINED BYTE COUNT
3001
CODE LENGTH COUNTER

FIG. 3

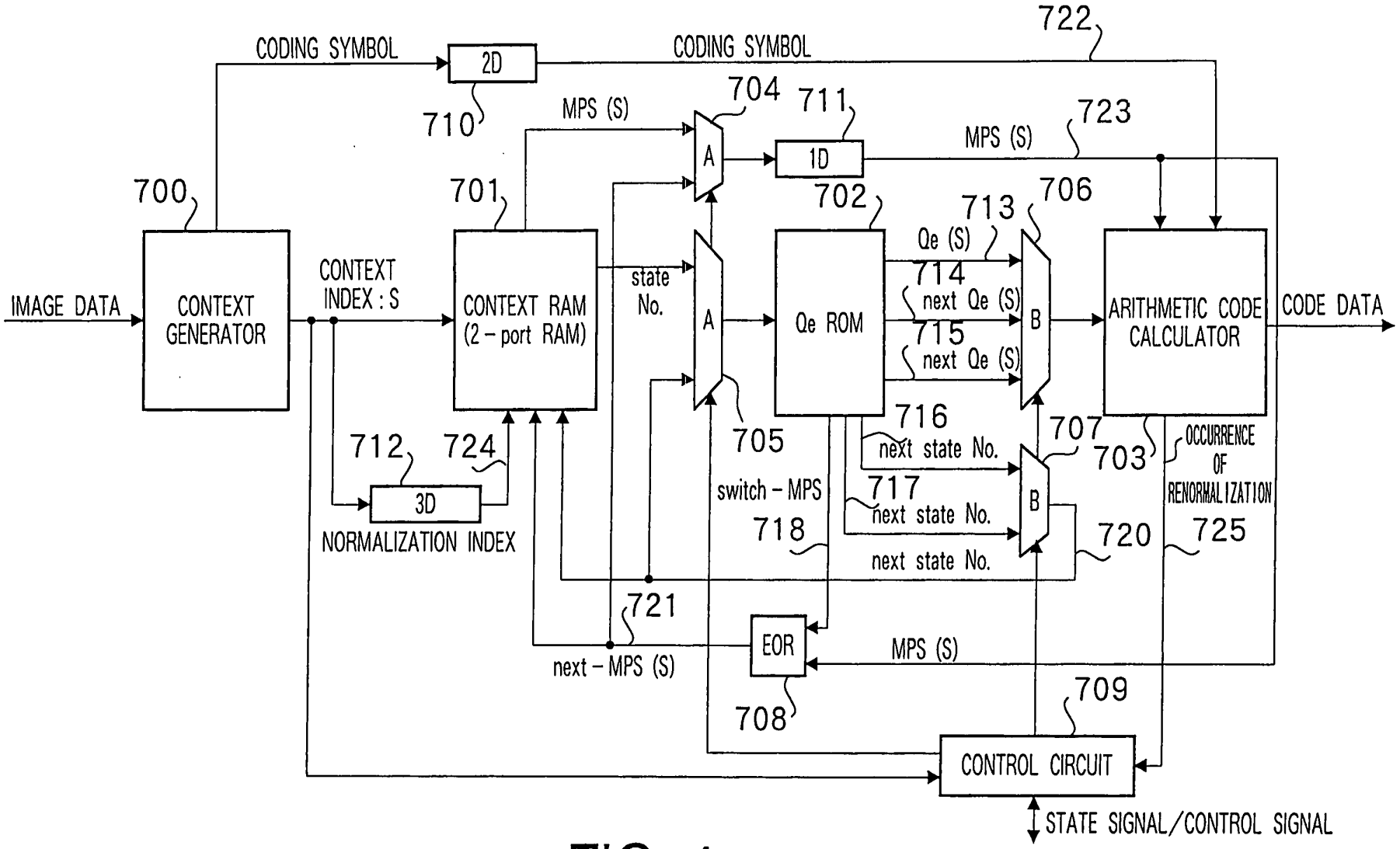
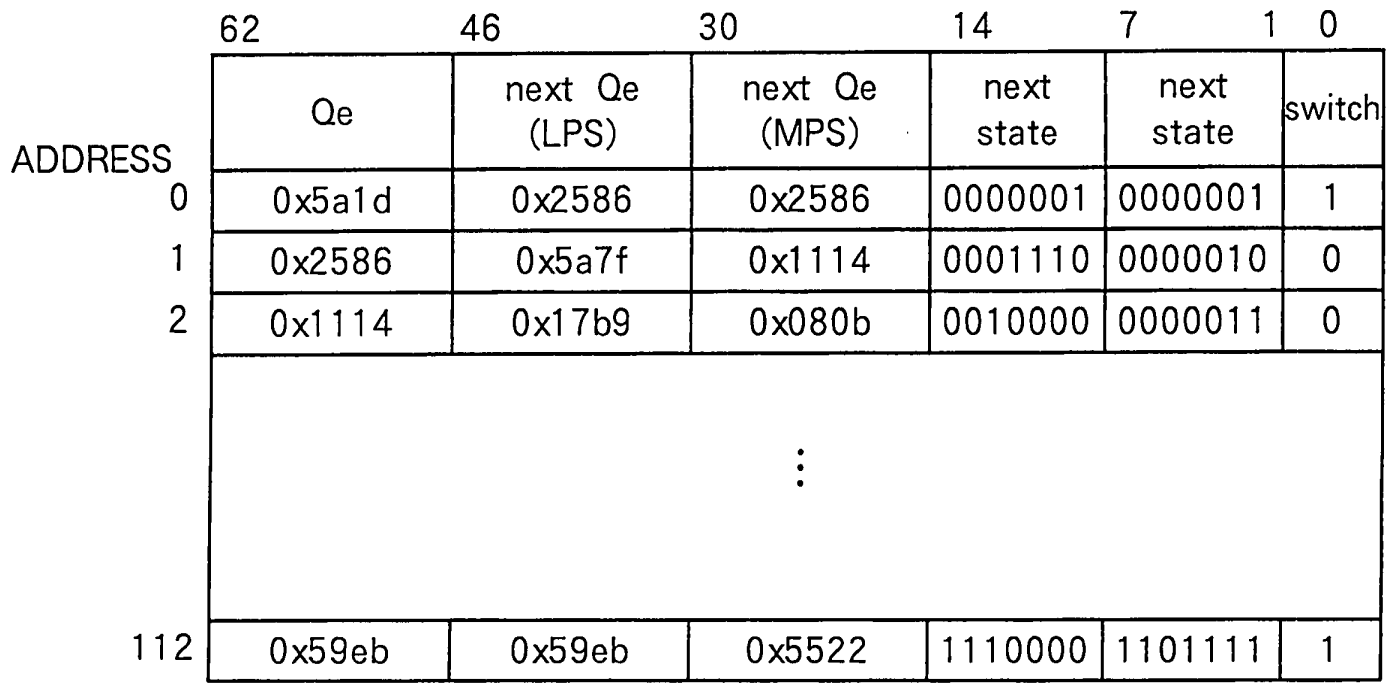

CODING SYMBOL
2D
CODING SYMBOL
722
710
MPS (S)
704
711
A
1D
MPS (S)
723
700
701
702
713
706
IMAGE DATA
CONTEXT GENERATOR
CONTEXT INDEX : S
CONTEXT RAM (2 – port RAM)
state No.
A
Qe ROM
Qe (S)
714
next Qe (S)
B
ARITHMETIC CODE CALCULATOR
CODE DATA
715
next Qe (S)
716
712
724
705
707
703
OCCURRENCE OF RENORMALIZATION
next state No.
switch – MPS
717
B
3D
NORMALIZATION INDEX
718
next state No.
720
725
next state No.
721
EOR
MPS (S)
next – MPS (S)
708
709
CONTROL CIRCUIT
STATE SIGNAL/CONTROL SIGNAL

FIG. 4



ADDRESS	62 Qe	46 next Qe (LPS)	30 next Qe (MPS)	14 next state	7 next state	1 switch	0
0	0x5a1d	0x2586	0x2586	0000001	0000001	1	
1	0x2586	0x5a7f	0x1114	0001110	0000010	0	
2	0x1114	0x17b9	0x080b	0010000	0000011	0	
	⋮						
112	0x59eb	0x59eb	0x5522	1110000	1101111	1	

FIG. 5

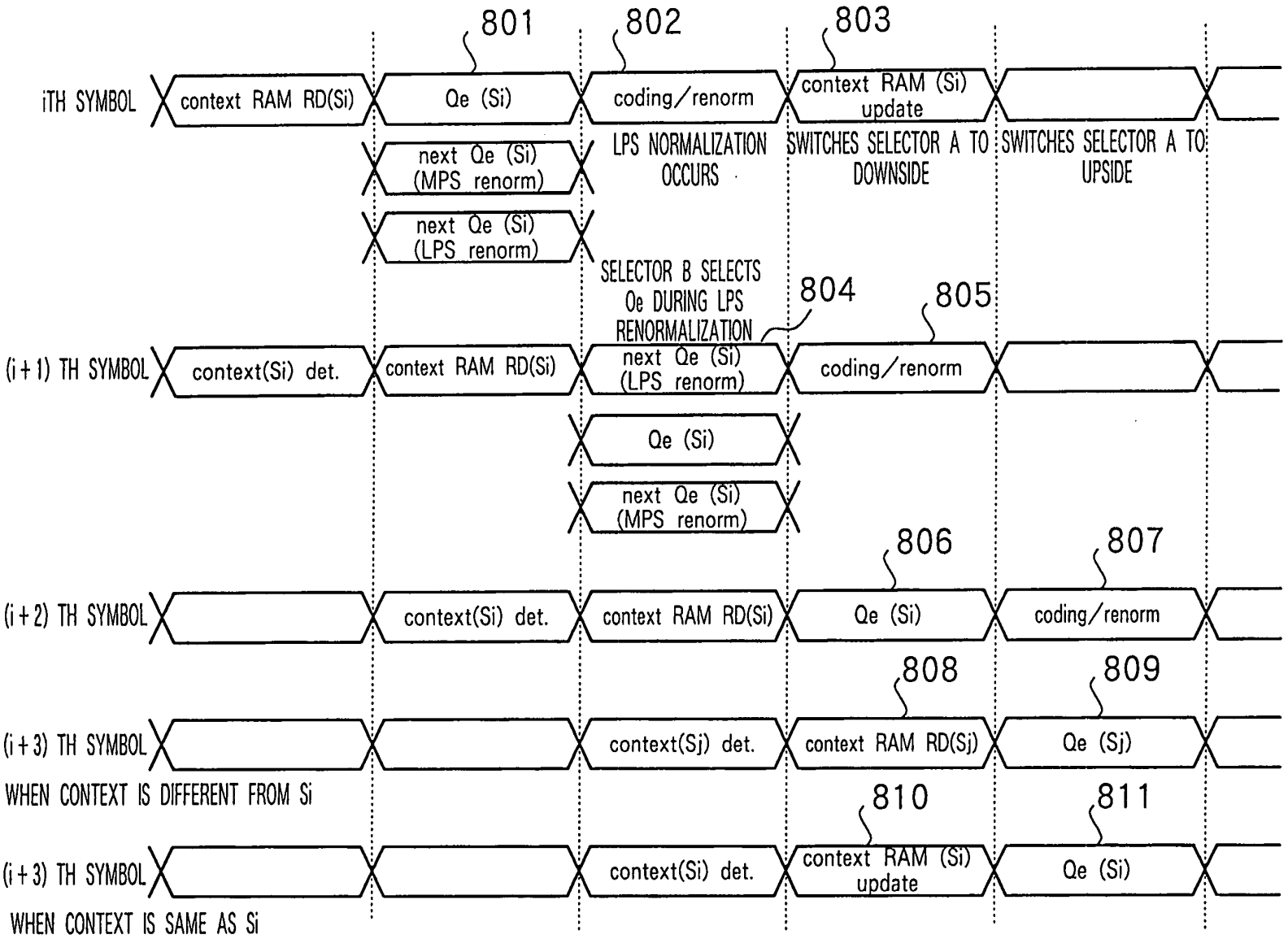

801
802
803
iTH SYMBOL
context RAM RD(Si)
Qe (Si)
coding/renorm
context RAM (Si) update
next Qe (Si) (MPS renorm)
LPS NORMALIZATION OCCURS
SWITCHES SELECTOR A TO DOWNSIDE
SWITCHES SELECTOR A TO UPSIDE
next Qe (Si) (LPS renorm)
SELECTOR B SELECTS Qe DURING LPS RENORMALIZATION
804
805
(i+1) TH SYMBOL
context(Si) det.
context RAM RD(Si)
next Qe (Si) (LPS renorm)
coding/renorm
Qe (Si)
next Qe (Si) (MPS renorm)
806
807
(i+2) TH SYMBOL
context(Si) det.
context RAM RD(Si)
Qe (Si)
coding/renorm
808
809
(i+3) TH SYMBOL
context(Sj) det.
context RAM RD(Sj)
Qe (Sj)
WHEN CONTEXT IS DIFFERENT FROM Si
810
811
(i+3) TH SYMBOL
context(Si) det.
context RAM (Si) update
Qe (Si)
WHEN CONTEXT IS SAME AS Si

FIG. 6

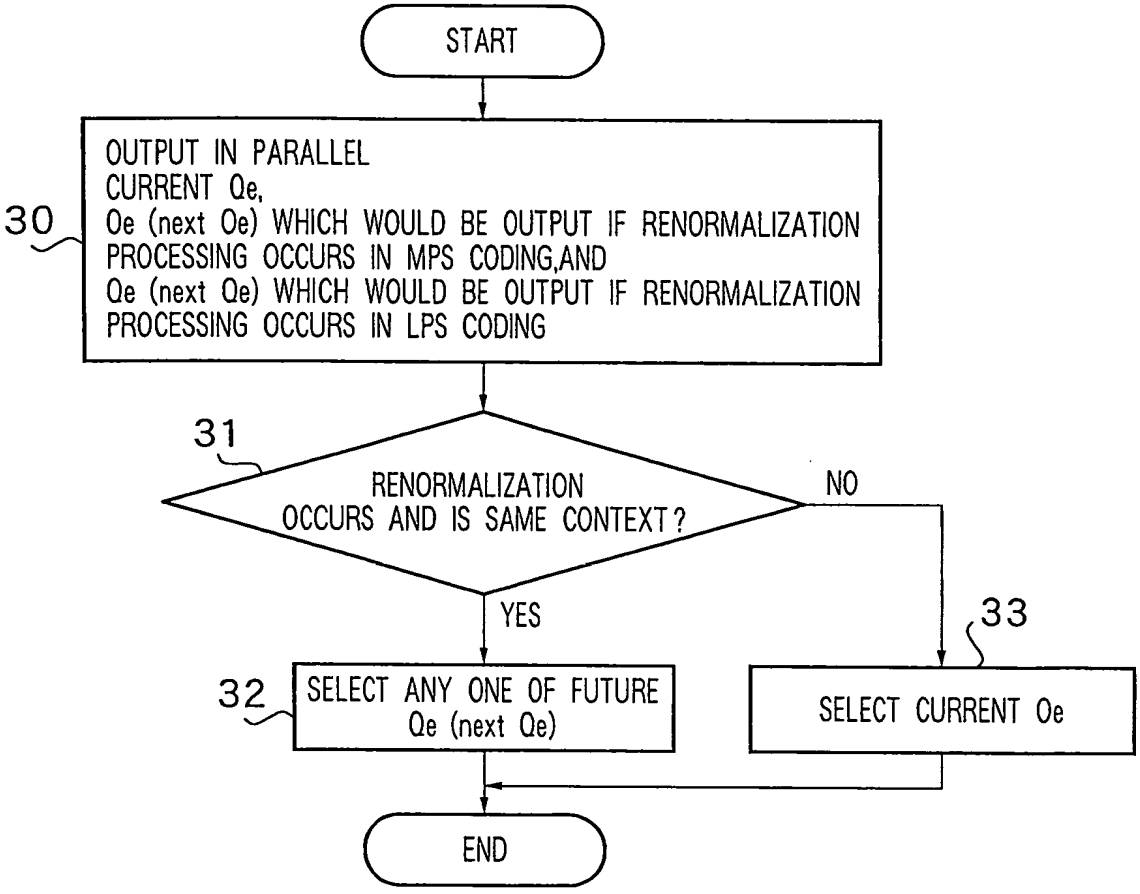

START
OUTPUT IN PARALLEL
CURRENT Qe,
Qe (next Qe) WHICH WOULD BE OUTPUT IF RENORMALIZATION PROCESSING OCCURS IN MPS CODING,AND
Qe (next Qe) WHICH WOULD BE OUTPUT IF RENORMALIZATION PROCESSING OCCURS IN LPS CODING
30
31
RENORMALIZATION OCCURS AND IS SAME CONTEXT?
NO
YES
33
32
SELECT ANY ONE OF FUTURE Qe (next Qe)
SELECT CURRENT Qe
END

FIG. 7

	DC COMPONENT			AC COMPONENT			
SYMBOL	T_{00},	T_{01}, ...,	T_{0i}	T_{10},	T_{11}, ...,	T_{1i}	.....
CONTEXT	S_{00},	S_{01}, ...,	S_{0i}	S_{10},	S_{11}, ...,	S_{1i}	.....

FIG. 8A

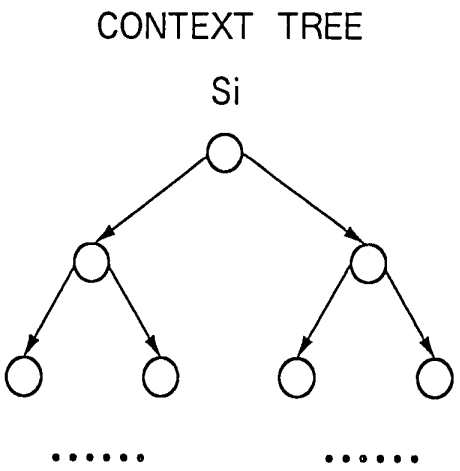


FIG. 8B

	DC COMPONENT			AC COMPONENT			
SYMBOL	T_{00},	T_{01}, ...,	T_{0i}	T_{10},	T_{11}, ...,	T_{1i}	.....
CONTEXT	S_{00},	S_{01}, ...,	S_{0i}	S_{10},	S_{11}, ...,	S_{1i}	.....

FIG. 9A

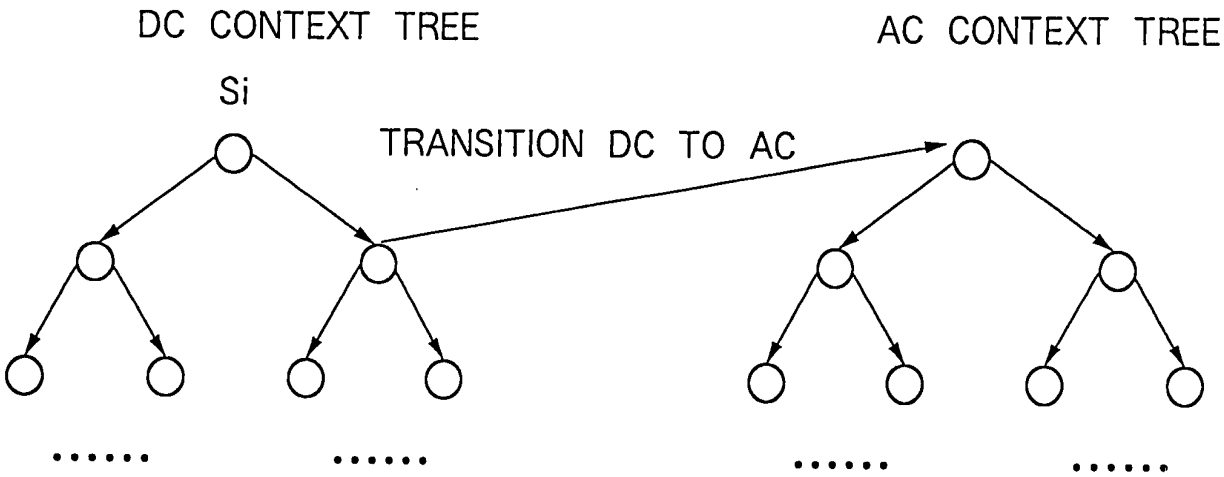


FIG. 9B

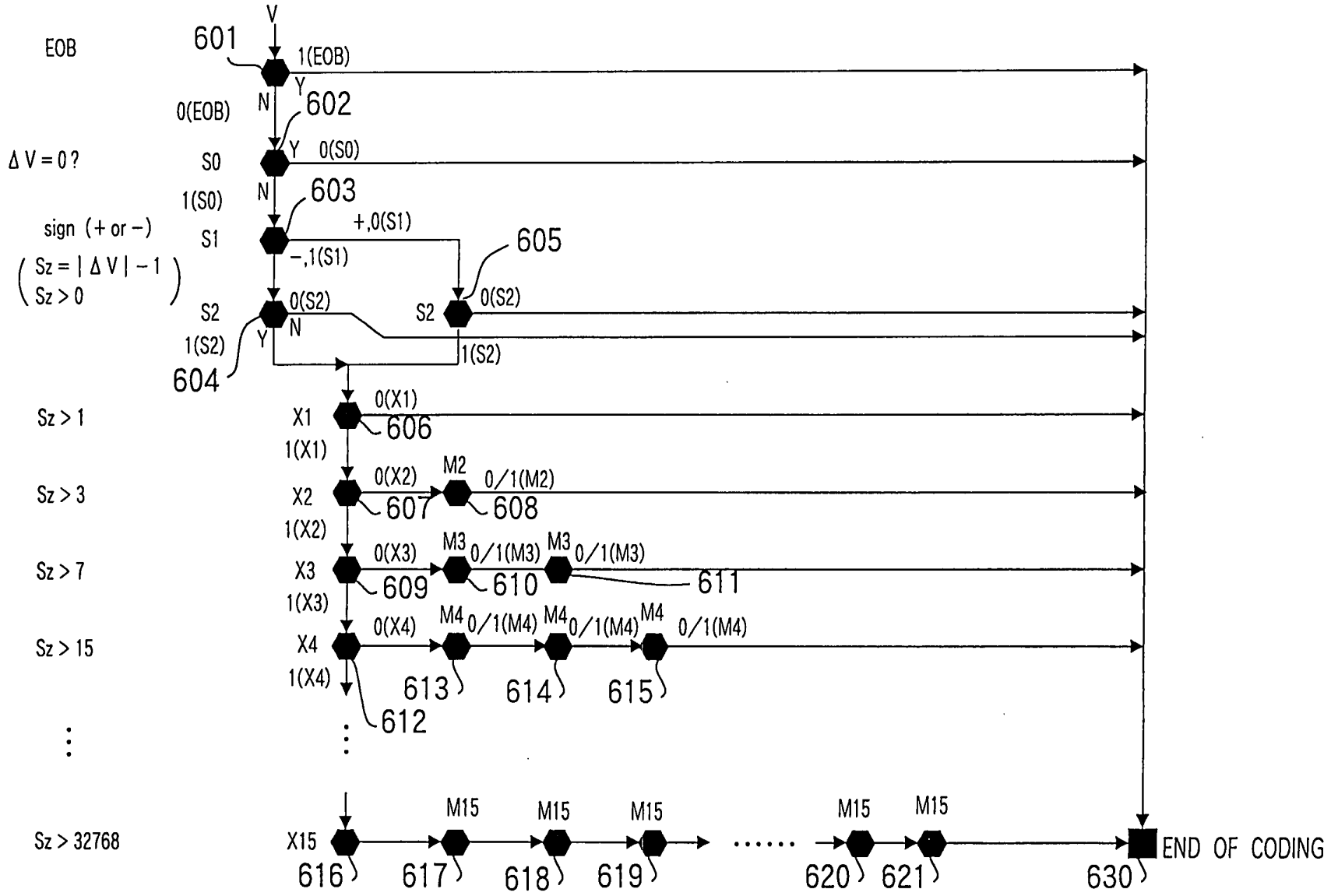

EOB
601
V
1(EOB)
Y
N
602
0(EOB)
ΔV = 0?
S0
Y
0(S0)
N
603
1(S0)
sign (+ or −)
S1
+,0(S1)
−,1(S1)
605
(Sz = | ΔV | − 1
Sz > 0)
S2
0(S2)
S2
0(S2)
N
Y
1(S2)
1(S2)
604
Sz > 1
X1
0(X1)
606
1(X1)
Sz > 3
X2
0(X2)
M2
0/1(M2)
607
608
1(X2)
Sz > 7
X3
0(X3)
M3
0/1(M3)
M3
0/1(M3)
609
610
611
1(X3)
Sz > 15
X4
0(X4)
M4
0/1(M4)
M4
0/1(M4)
M4
0/1(M4)
613
614
615
1(X4)
612
Sz > 32768
X15
M15
M15
M15
M15
M15
616
617
618
619
620
621
630
END OF CODING

FIG. 10

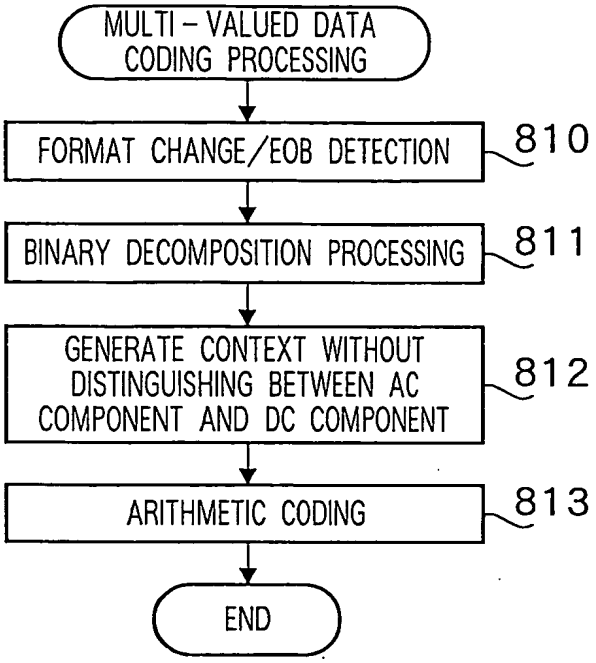


FIG. 11A

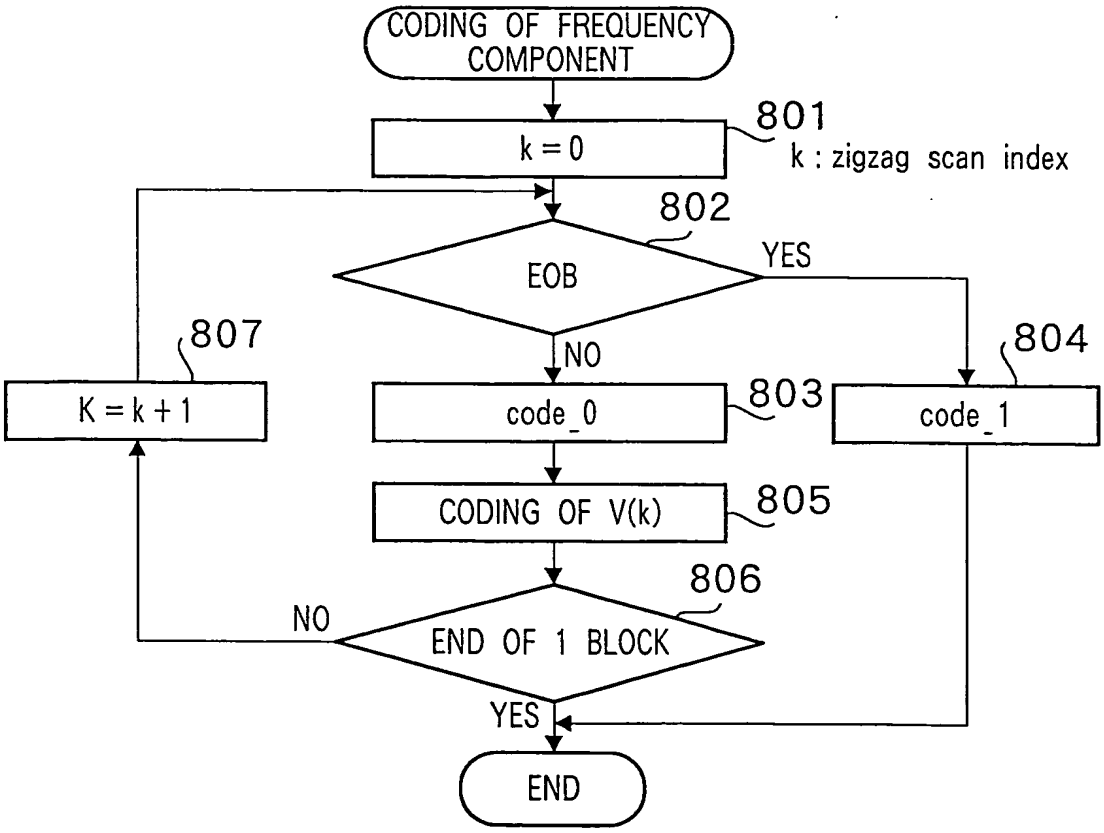


FIG. 11B

FIG. 12A

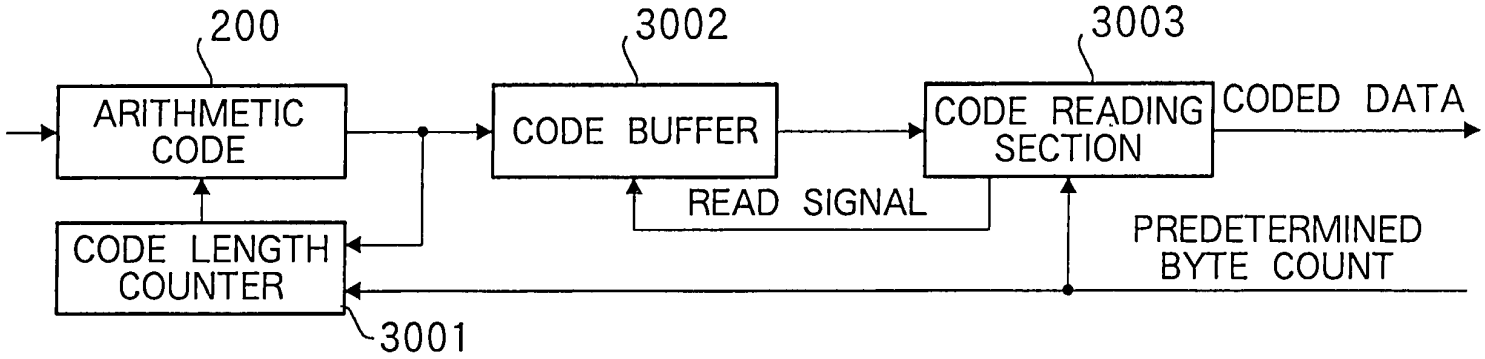


FIG. 12B

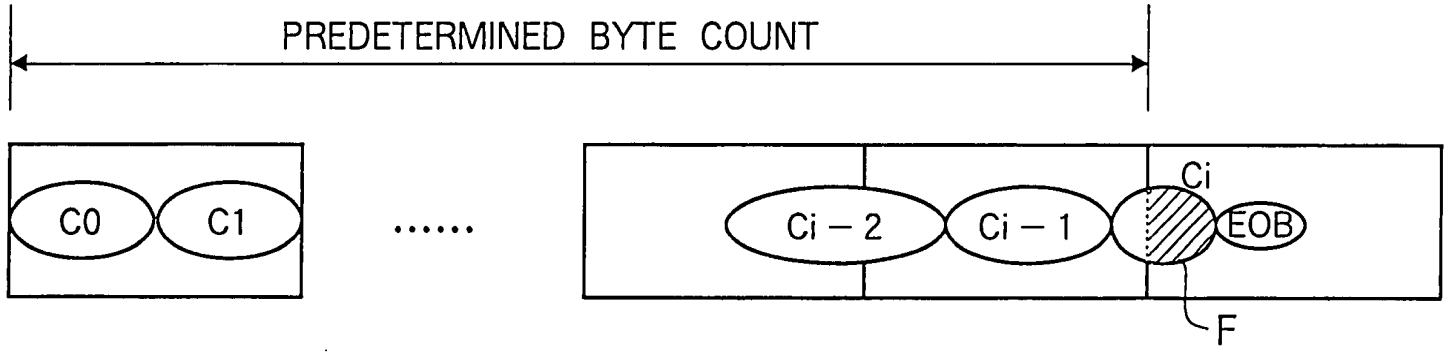
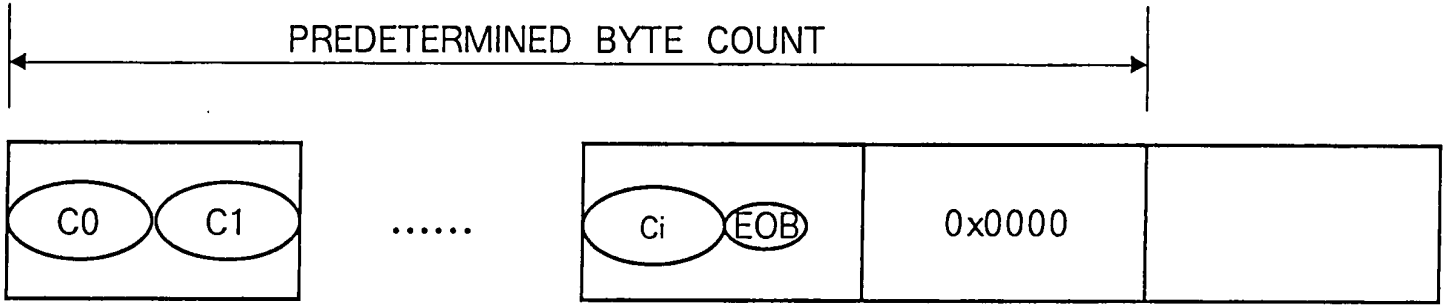


FIG. 12C



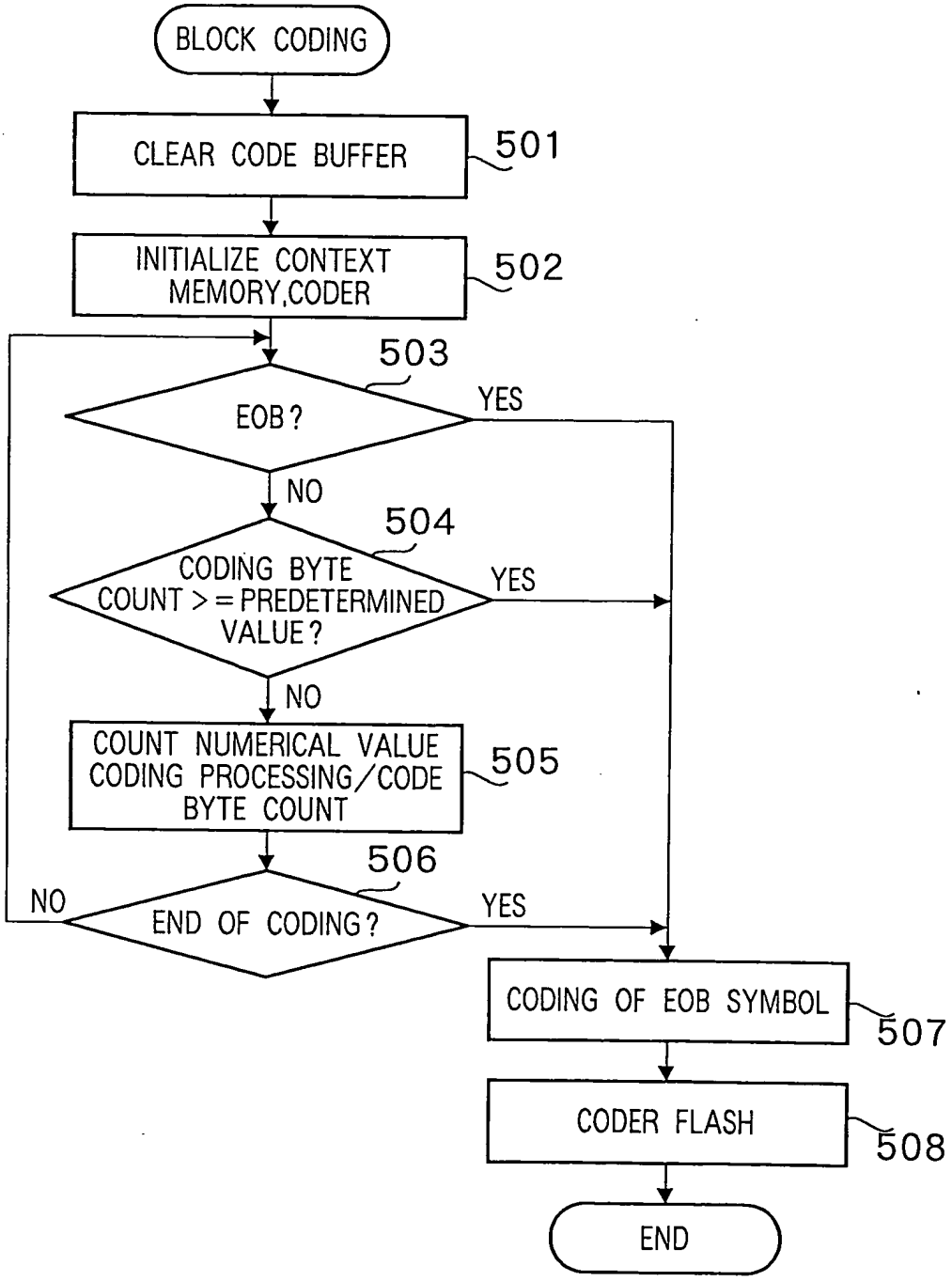

BLOCK CODING
CLEAR CODE BUFFER
501
INITIALIZE CONTEXT MEMORY,CODER
502
503
EOB?
YES
NO
504
CODING BYTE COUNT >= PREDETERMINED VALUE?
YES
NO
COUNT NUMERICAL VALUE CODING PROCESSING/CODE BYTE COUNT
505
506
NO
END OF CODING?
YES
CODING OF EOB SYMBOL
507
CODER FLASH
508
END

FIG. 13

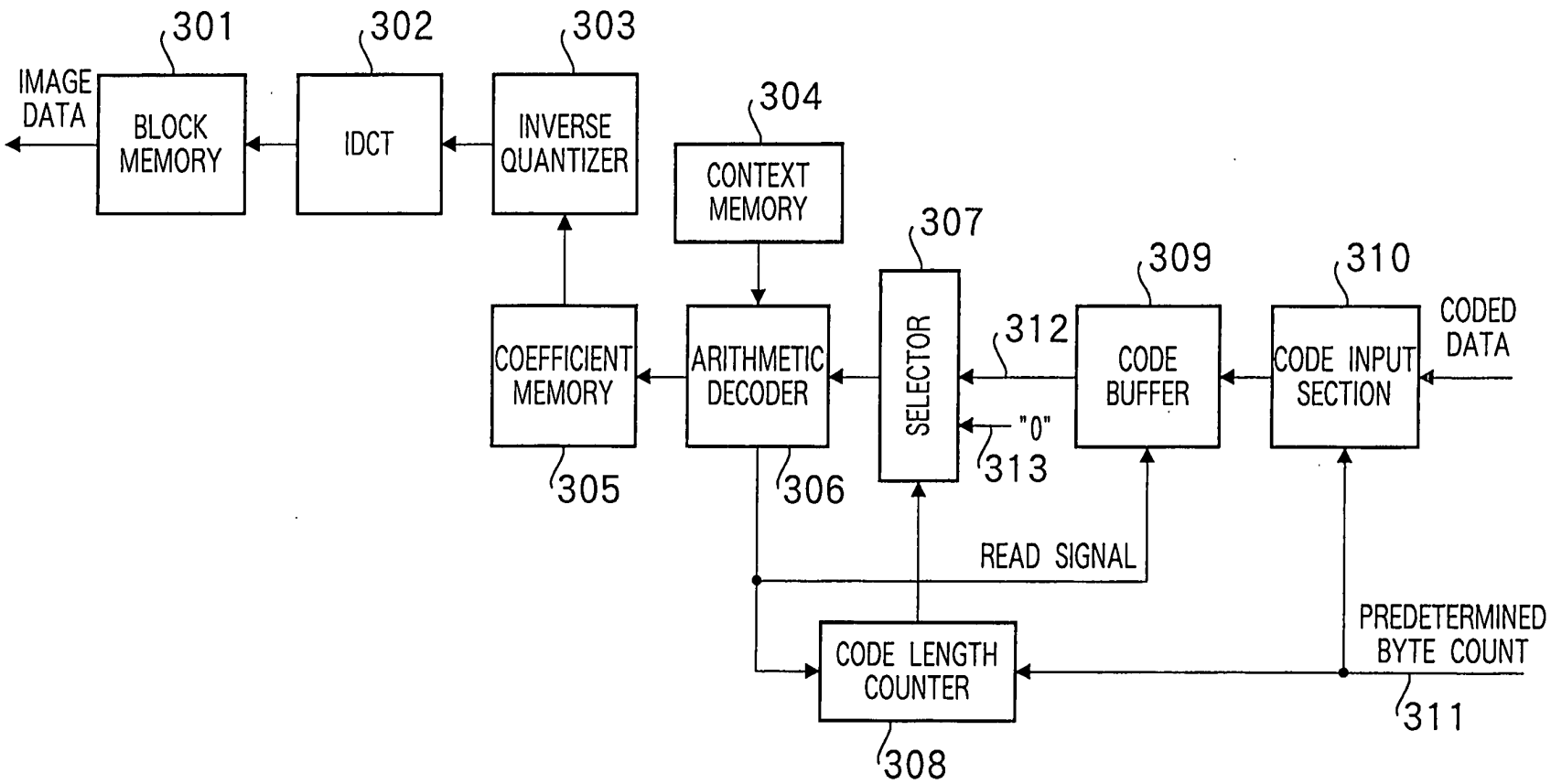

301
302
303
IMAGE DATA
BLOCK MEMORY
IDCT
INVERSE QUANTIZER
304
CONTEXT MEMORY
307
309
310
CODED DATA
312
COEFFICIENT MEMORY
ARITHMETIC DECODER
SELECTOR
CODE BUFFER
CODE INPUT SECTION
"0"
313
305
306
READ SIGNAL
PREDETERMINED BYTE COUNT
CODE LENGTH COUNTER
311
308

FIG. 14

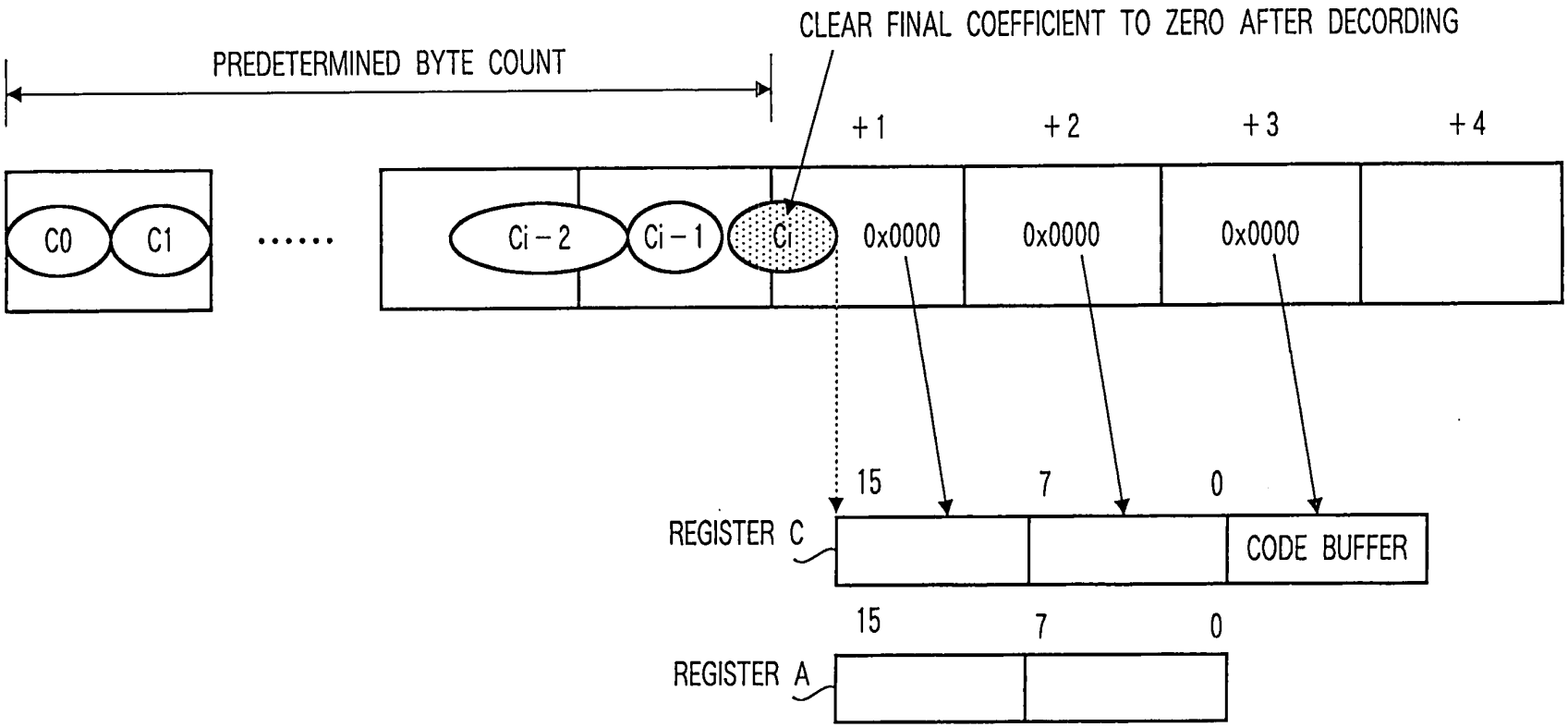

CLEAR FINAL COEFFICIENT TO ZERO AFTER DECORDING
PREDETERMINED BYTE COUNT
+1
+2
+3
+4
C0
C1
.....
Ci-2
Ci-1
Ci
0x0000
0x0000
0x0000
15
7
0
REGISTER C
CODE BUFFER
15
7
0
REGISTER A

FIG. 15

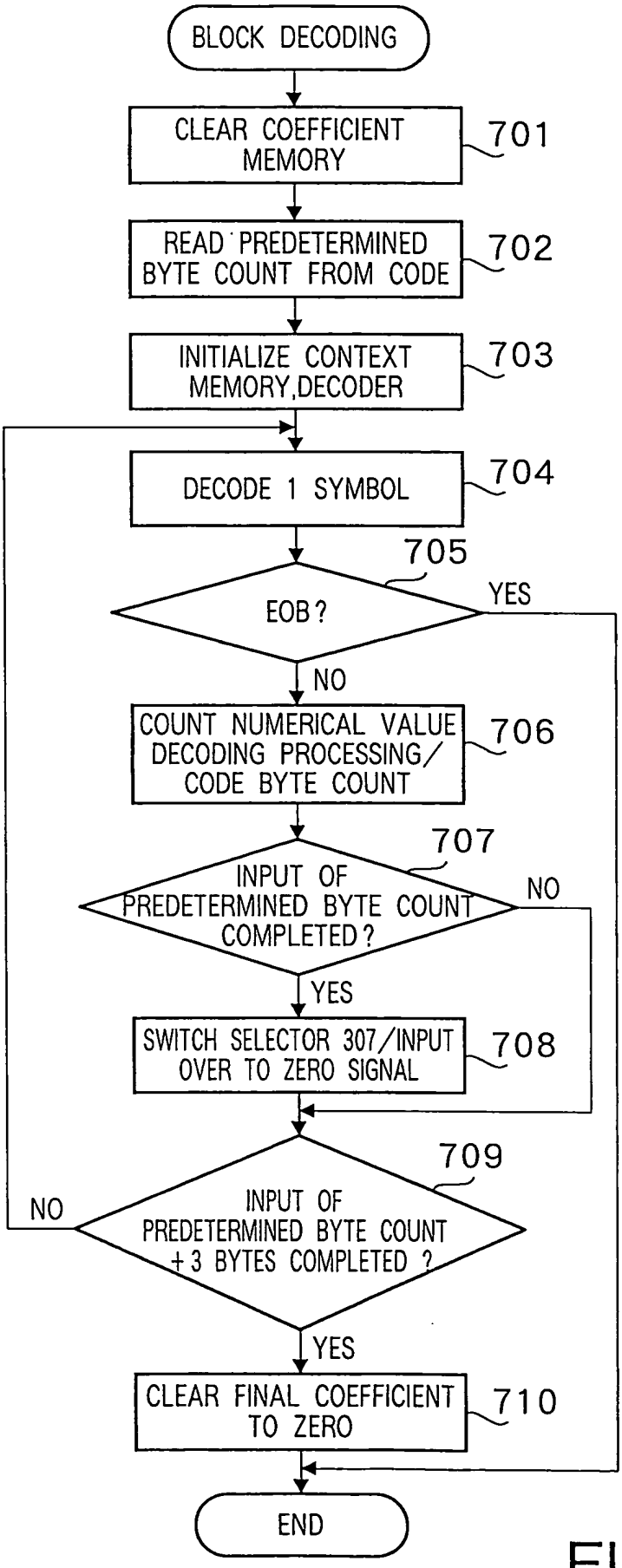

BLOCK DECODING
CLEAR COEFFICIENT MEMORY
701
READ PREDETERMINED BYTE COUNT FROM CODE
702
INITIALIZE CONTEXT MEMORY,DECODER
703
DECODE 1 SYMBOL
704
705
EOB?
YES
NO
COUNT NUMERICAL VALUE DECODING PROCESSING/ CODE BYTE COUNT
706
707
INPUT OF PREDETERMINED BYTE COUNT COMPLETED?
NO
YES
SWITCH SELECTOR 307/INPUT OVER TO ZERO SIGNAL
708
709
NO
INPUT OF PREDETERMINED BYTE COUNT +3 BYTES COMPLETED ?
YES
CLEAR FINAL COEFFICIENT TO ZERO
710
END

FIG. 16

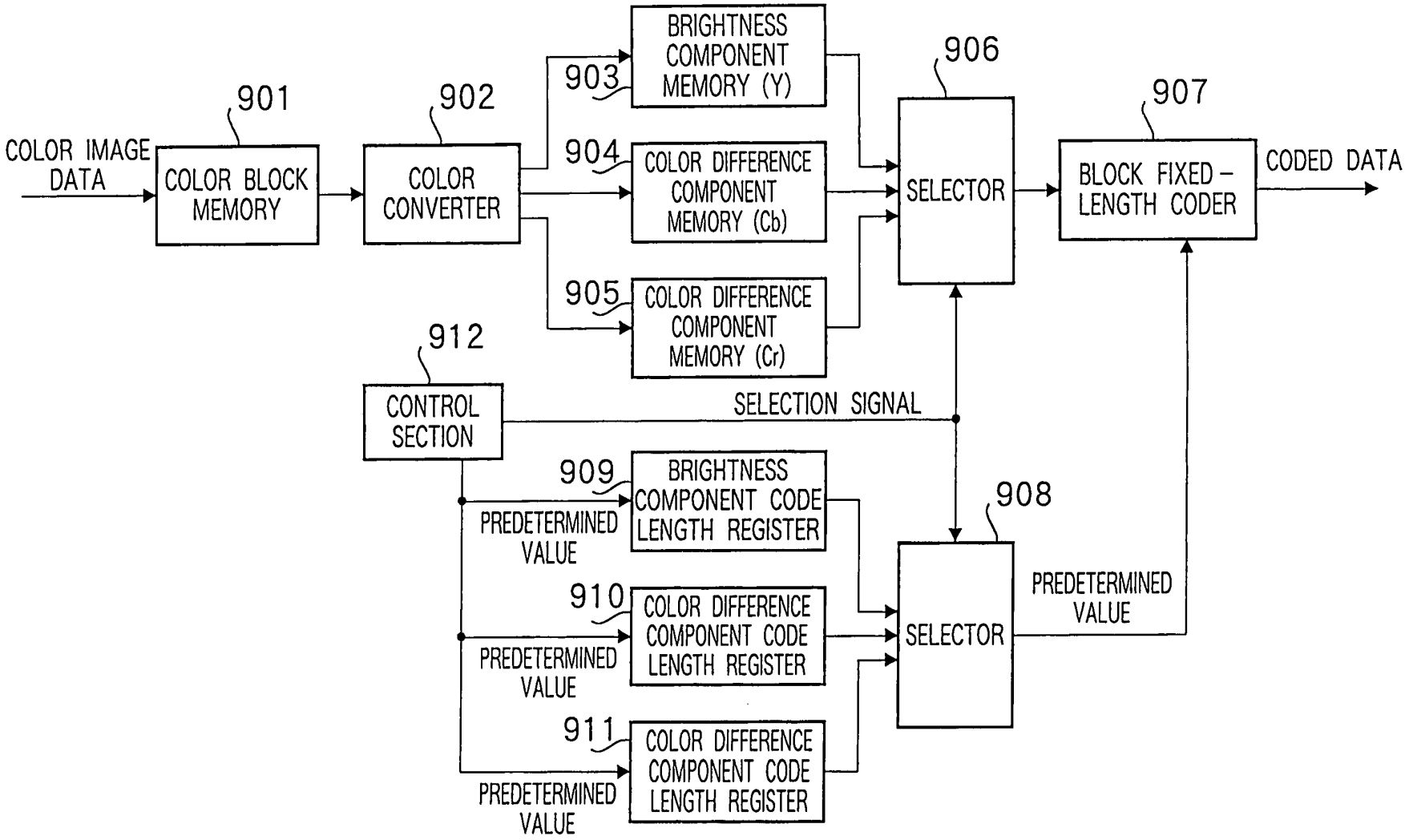

COLOR IMAGE DATA
901
COLOR BLOCK MEMORY
902
COLOR CONVERTER
903
BRIGHTNESS COMPONENT MEMORY (Y)
904
COLOR DIFFERENCE COMPONENT MEMORY (Cb)
905
COLOR DIFFERENCE COMPONENT MEMORY (Cr)
906
SELECTOR
907
BLOCK FIXED – LENGTH CODER
CODED DATA
912
CONTROL SECTION
SELECTION SIGNAL
909
BRIGHTNESS COMPONENT CODE LENGTH REGISTER
PREDETERMINED VALUE
910
COLOR DIFFERENCE COMPONENT CODE LENGTH REGISTER
PREDETERMINED VALUE
911
COLOR DIFFERENCE COMPONENT CODE LENGTH REGISTER
PREDETERMINED VALUE
908
SELECTOR
PREDETERMINED VALUE

FIG. 17

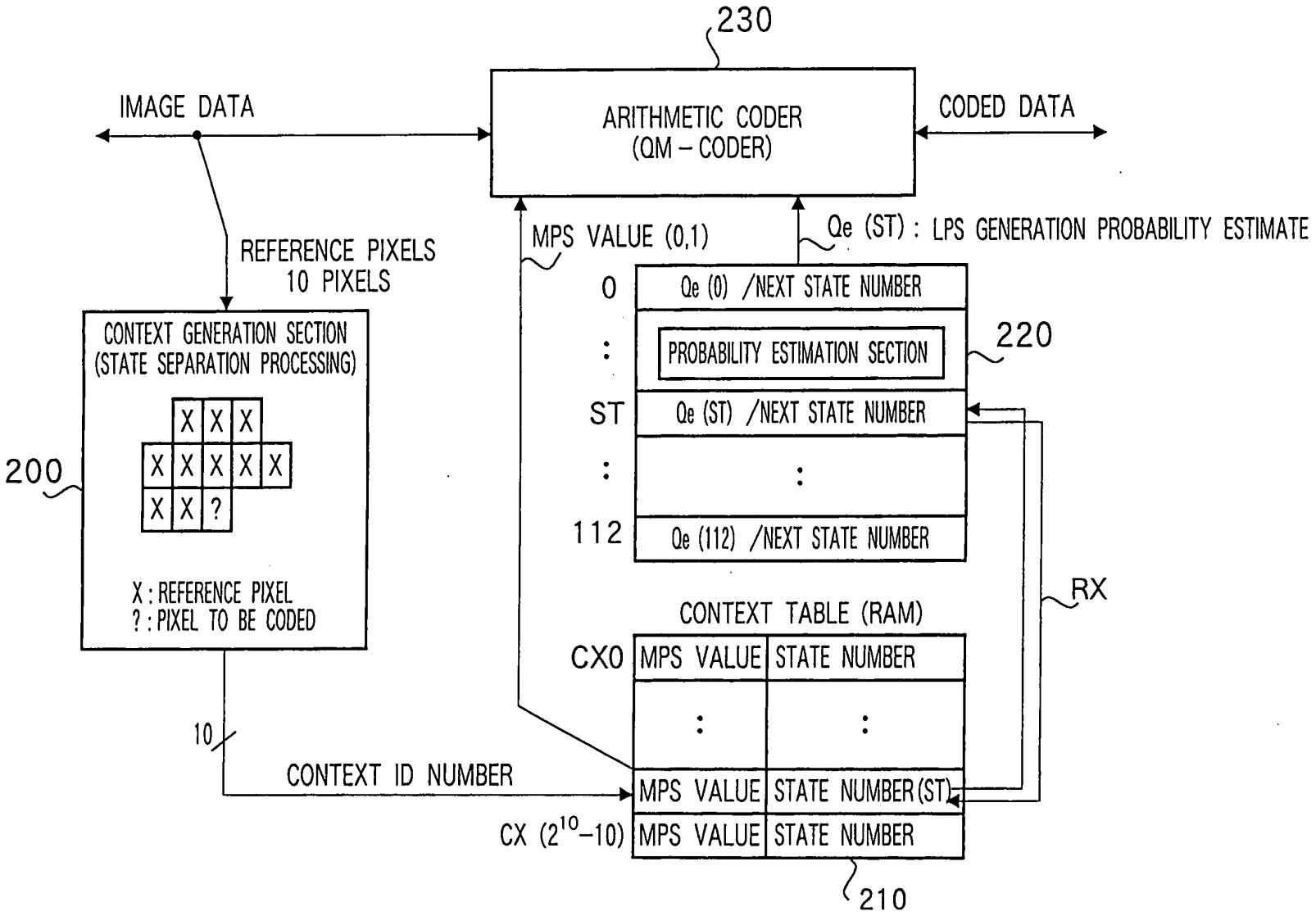

230
IMAGE DATA
ARITHMETIC CODER
(QM – CODER)
CODED DATA
REFERENCE PIXELS
10 PIXELS
MPS VALUE (0,1)
Qe (ST) : LPS GENERATION PROBABILITY ESTIMATE
0
Qe (0) /NEXT STATE NUMBER
PROBABILITY ESTIMATION SECTION
220
ST
Qe (ST) /NEXT STATE NUMBER
112
Qe (112) /NEXT STATE NUMBER
CONTEXT GENERATION SECTION
(STATE SEPARATION PROCESSING)
200
X : REFERENCE PIXEL
? : PIXEL TO BE CODED
RX
CONTEXT TABLE (RAM)
CX0
MPS VALUE
STATE NUMBER
10
CONTEXT ID NUMBER
MPS VALUE
STATE NUMBER (ST)
CX (2^10–10)
MPS VALUE
STATE NUMBER
210

FIG. 18

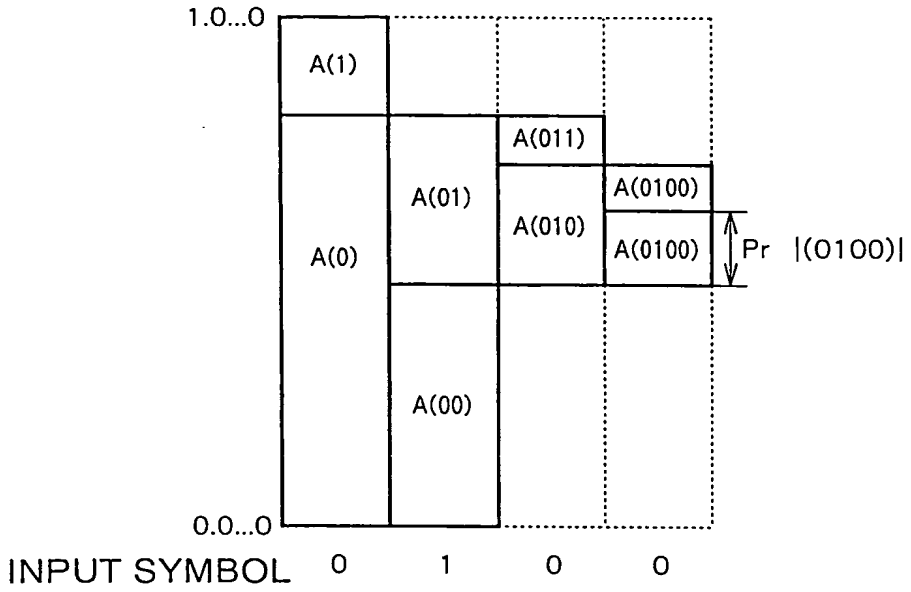

1.0...0
A(1)
A(011)
A(0100)
A(01)
A(010)
A(0100)
Pr |(0100)|
A(0)
A(00)
0.0...0
INPUT SYMBOL
0
1
0
0

FIG. 19

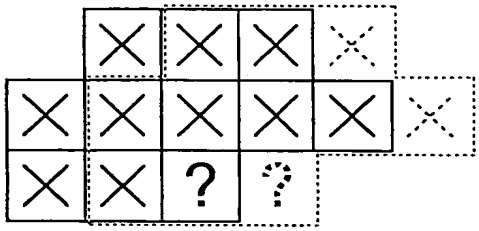


FIG. 20

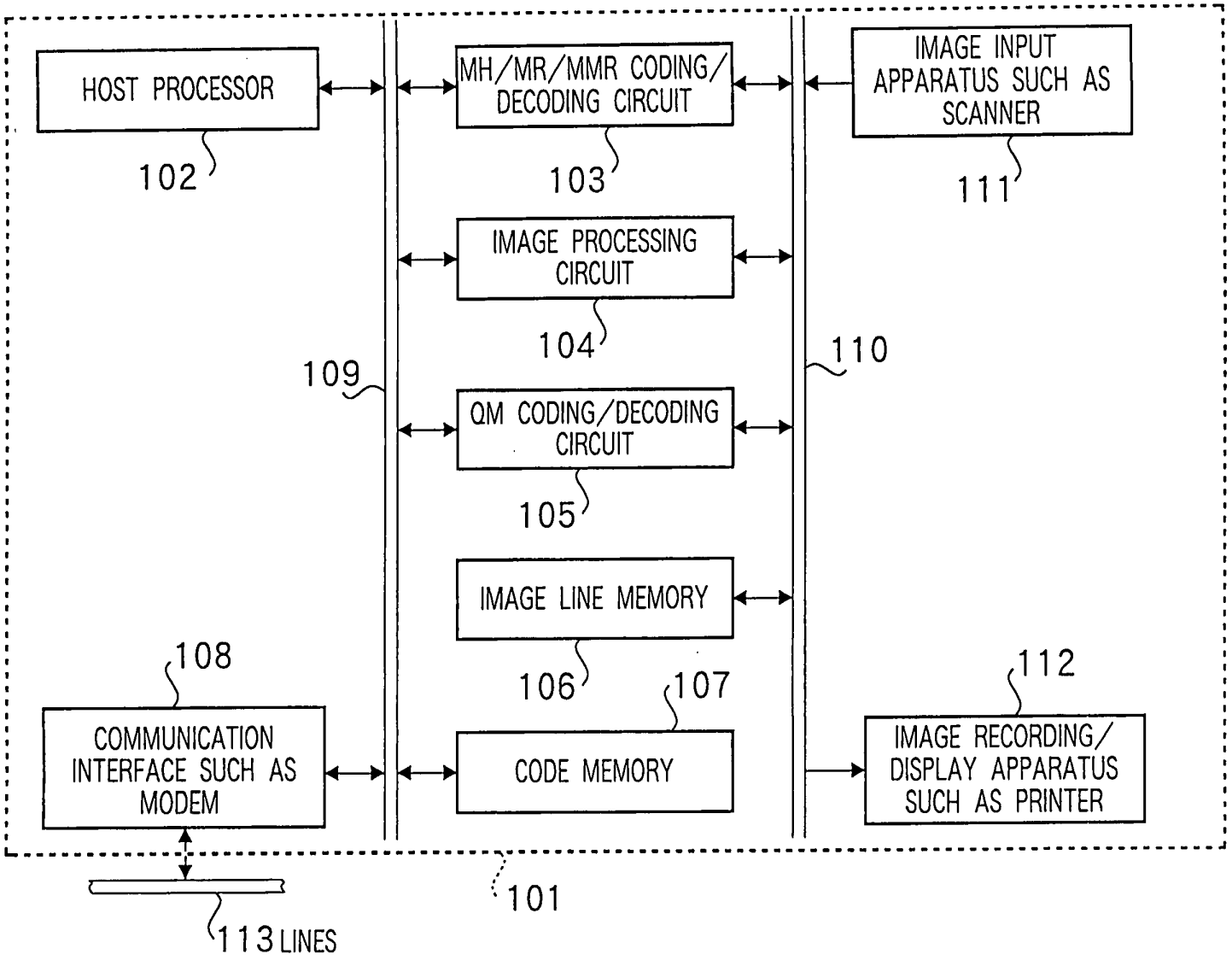

HOST PROCESSOR
102
MH/MR/MMR CODING/
DECODING CIRCUIT
103
IMAGE INPUT
APPARATUS SUCH AS
SCANNER
111
IMAGE PROCESSING
CIRCUIT
104
109
110
QM CODING/DECODING
CIRCUIT
105
IMAGE LINE MEMORY
106
108
107
112
COMMUNICATION
INTERFACE SUCH AS
MODEM
CODE MEMORY
IMAGE RECORDING/
DISPLAY APPARATUS
SUCH AS PRINTER
101
113 LINES

FIG. 21

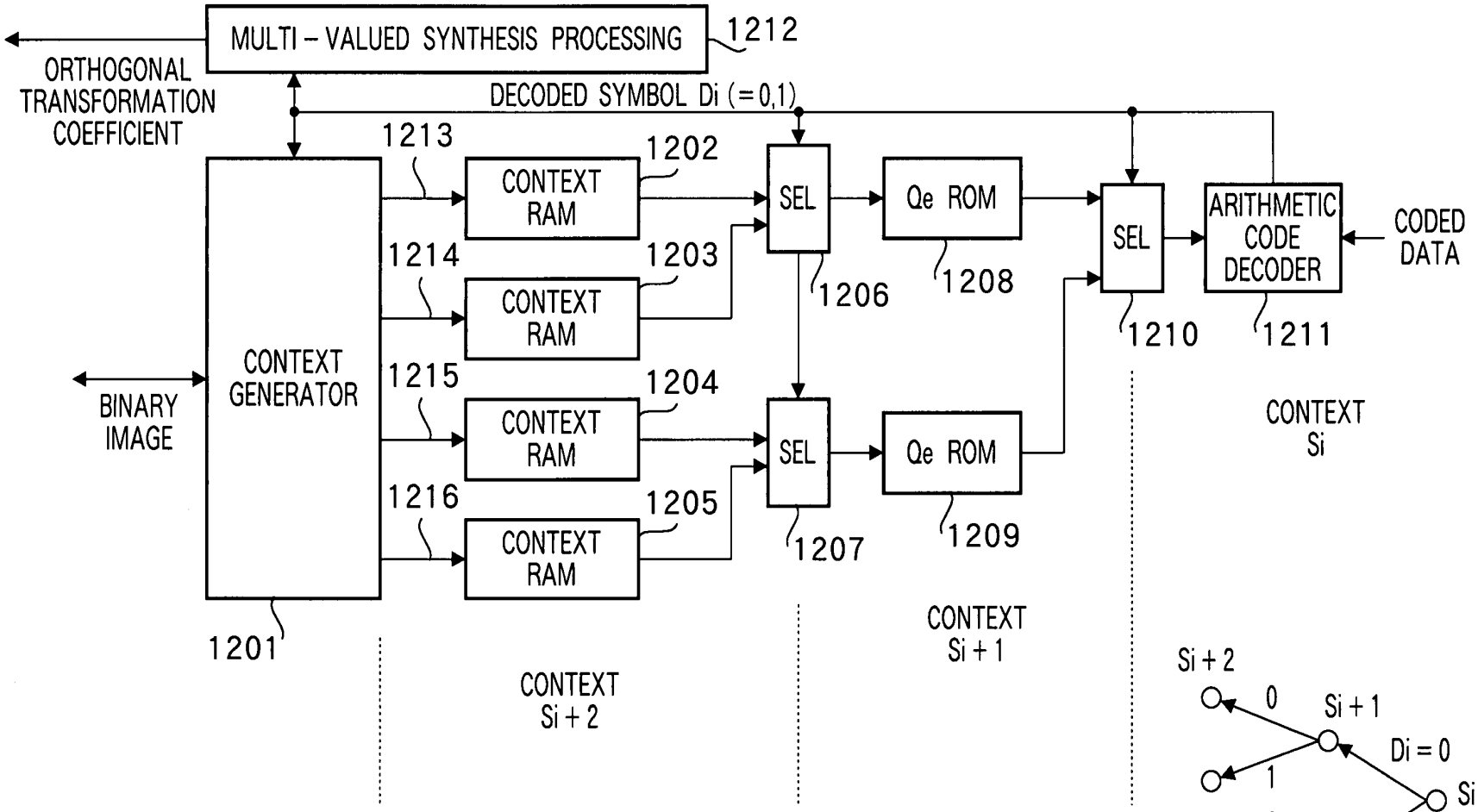

MULTI – VALUED SYNTHESIS PROCESSING
1212
ORTHOGONAL TRANSFORMATION COEFFICIENT
DECODED SYMBOL Di (=0,1)
1213
1214
1215
1216
CONTEXT RAM
CONTEXT RAM
CONTEXT RAM
CONTEXT RAM
1202
1203
1204
1205
SEL
SEL
1206
1207
Qe ROM
Qe ROM
1208
1209
SEL
1210
ARITHMETIC CODE DECODER
1211
CODED DATA
BINARY IMAGE
CONTEXT GENERATOR
1201
CONTEXT Si + 2
CONTEXT Si + 1
CONTEXT Si

FIG.22

Si + 2
0
Si + 1
Di = 0
1
Si
0
Di = 1
1

FIG.23

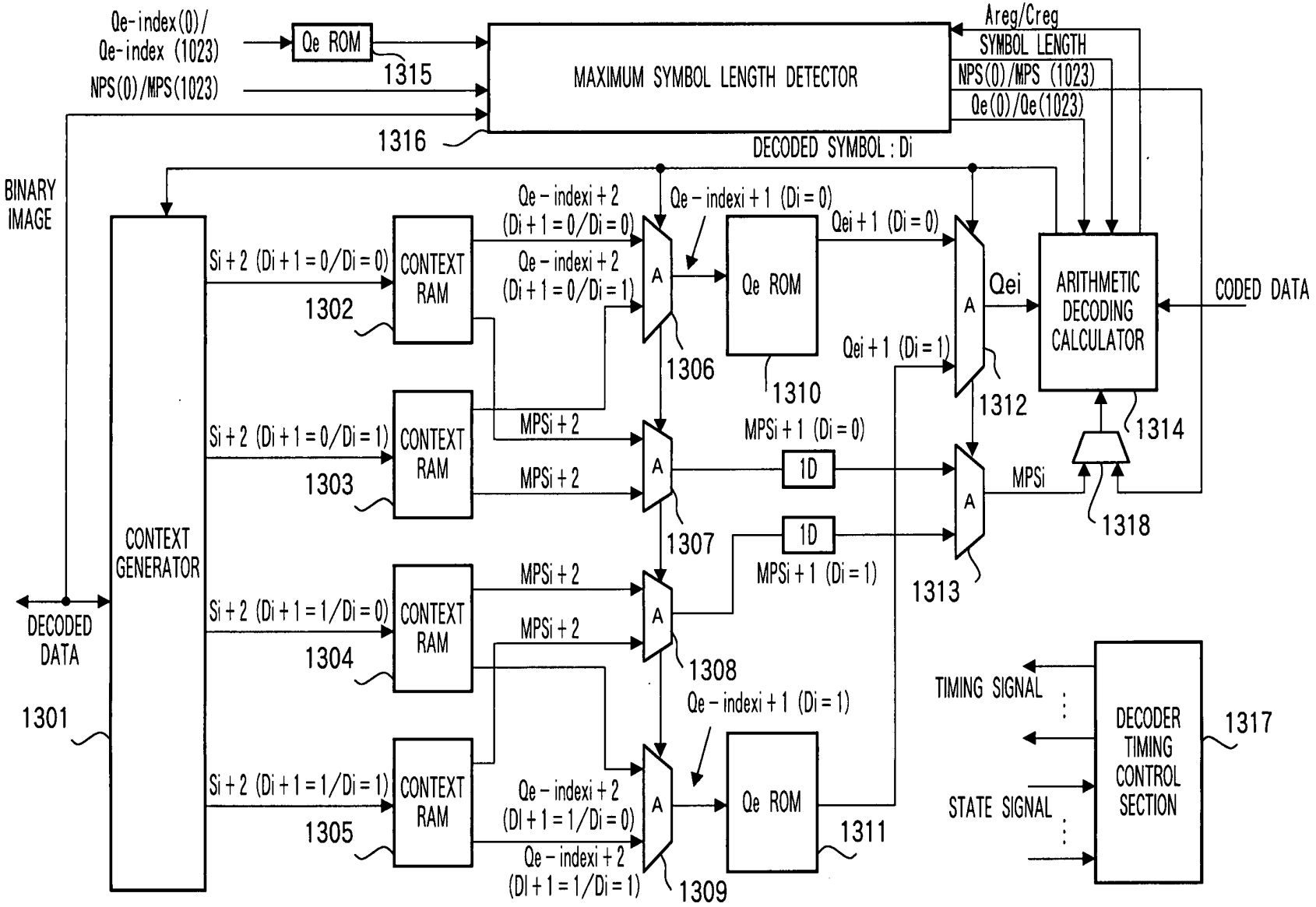

Qe-index(0)/
Qe-index (1023)
NPS(0)/MPS(1023)
Qe ROM
1315
MAXIMUM SYMBOL LENGTH DETECTOR
Areg/Creg
SYMBOL LENGTH
NPS(0)/MPS (1023)
Qe(0)/Qe(1023)
1316
DECODED SYMBOL : Di
BINARY IMAGE
CONTEXT GENERATOR
1301
DECODED DATA
Si + 2 (Di + 1 = 0/Di = 0)
Si + 2 (Di + 1 = 0/Di = 1)
Si + 2 (Di + 1 = 1/Di = 0)
Si + 2 (Di + 1 = 1/Di = 1)
CONTEXT RAM
1302
1303
1304
1305
Qe - indexi + 2 (Di + 1 = 0/Di = 0)
Qe - indexi + 2 (Di + 1 = 0/Di = 1)
Qe - indexi + 2 (DI + 1 = 1/Di = 0)
Qe - indexi + 2 (DI + 1 = 1/Di = 1)
Qe - indexi + 1 (Di = 0)
Qe - indexi + 1 (Di = 1)
A
1306
1307
1308
1309
Qe ROM
1310
1311
Qei + 1 (Di = 0)
Qei + 1 (Di = 1)
MPSi + 2
MPSi + 1 (Di = 0)
MPSi + 1 (Di = 1)
1D
Qei
MPSi
1312
1313
ARITHMETIC DECODING CALCULATOR
1314
1318
CODED DATA
TIMING SIGNAL
STATE SIGNAL
DECODER TIMING CONTROL SECTION
1317

FIG.24

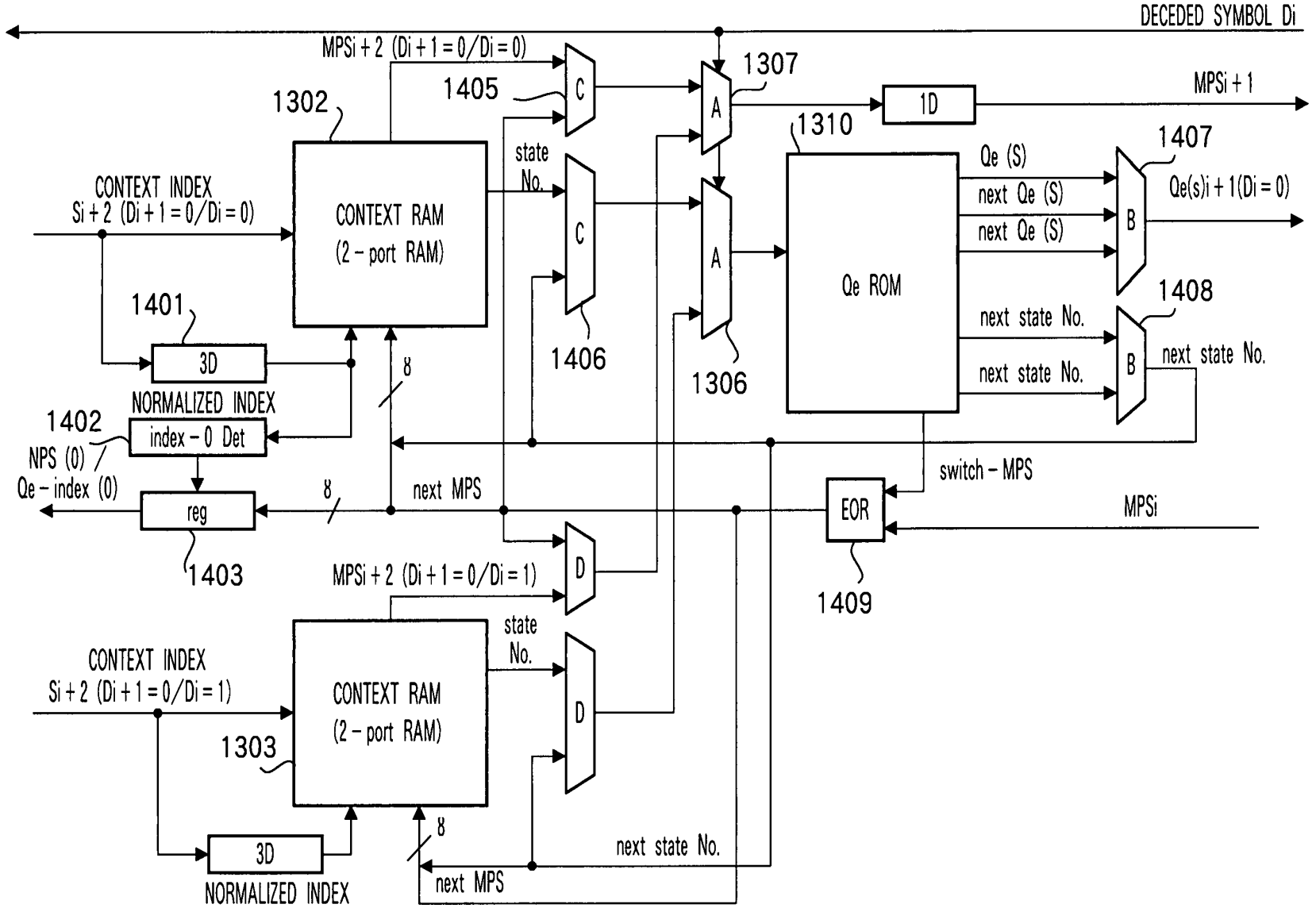

DECEDED SYMBOL Di
MPSi + 2 (Di + 1 = 0/Di = 0)
1405
C
1307
A
1D
MPSi + 1
1302
1310
1407
state No.
CONTEXT INDEX
Si + 2 (Di + 1 = 0/Di = 0)
CONTEXT RAM
(2 - port RAM)
C
A
Qe (S)
next Qe (S)
next Qe (S)
B
Qe(s)i + 1(Di = 0)
Qe ROM
1401
1408
next state No.
next state No.
B
next state No.
3D
1406
1306
8
NORMALIZED INDEX
1402
index - 0 Det
NPS (0) / Qe - index (0)
switch - MPS
8
next MPS
reg
EOR
MPSi
1403
1409
MPSi + 2 (Di + 1 = 0/Di = 1)
D
state No.
CONTEXT INDEX
Si + 2 (Di + 1 = 0/Di = 1)
CONTEXT RAM
(2 - port RAM)
1303
D
3D
8
next state No.
NORMALIZED INDEX
next MPS

FIG.25

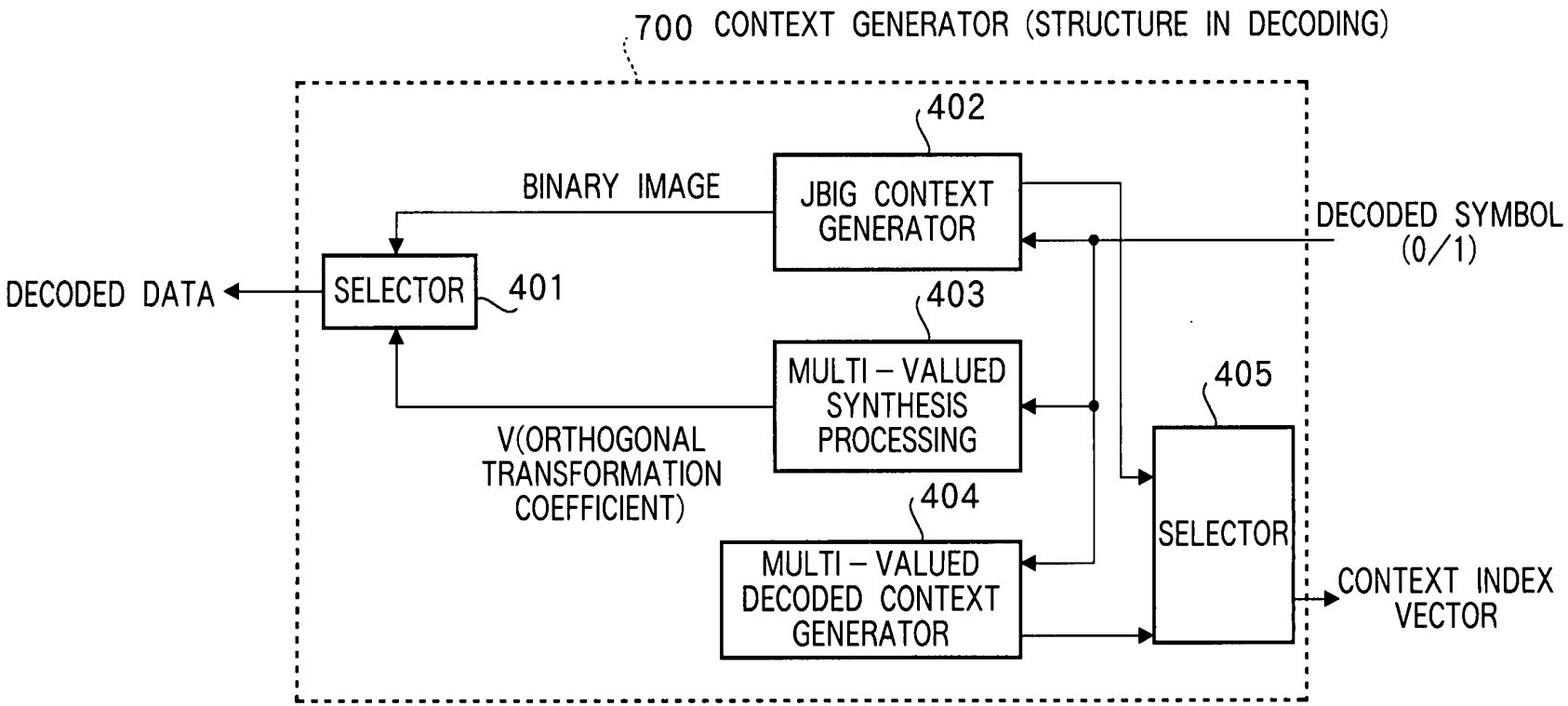

700 CONTEXT GENERATOR (STRUCTURE IN DECODING)
402
JBIG CONTEXT GENERATOR
BINARY IMAGE
DECODED SYMBOL (0/1)
DECODED DATA
SELECTOR
401
403
MULTI – VALUED SYNTHESIS PROCESSING
405
V(ORTHOGONAL TRANSFORMATION COEFFICIENT)
404
SELECTOR
MULTI – VALUED DECODED CONTEXT GENERATOR
CONTEXT INDEX VECTOR

FIG.26

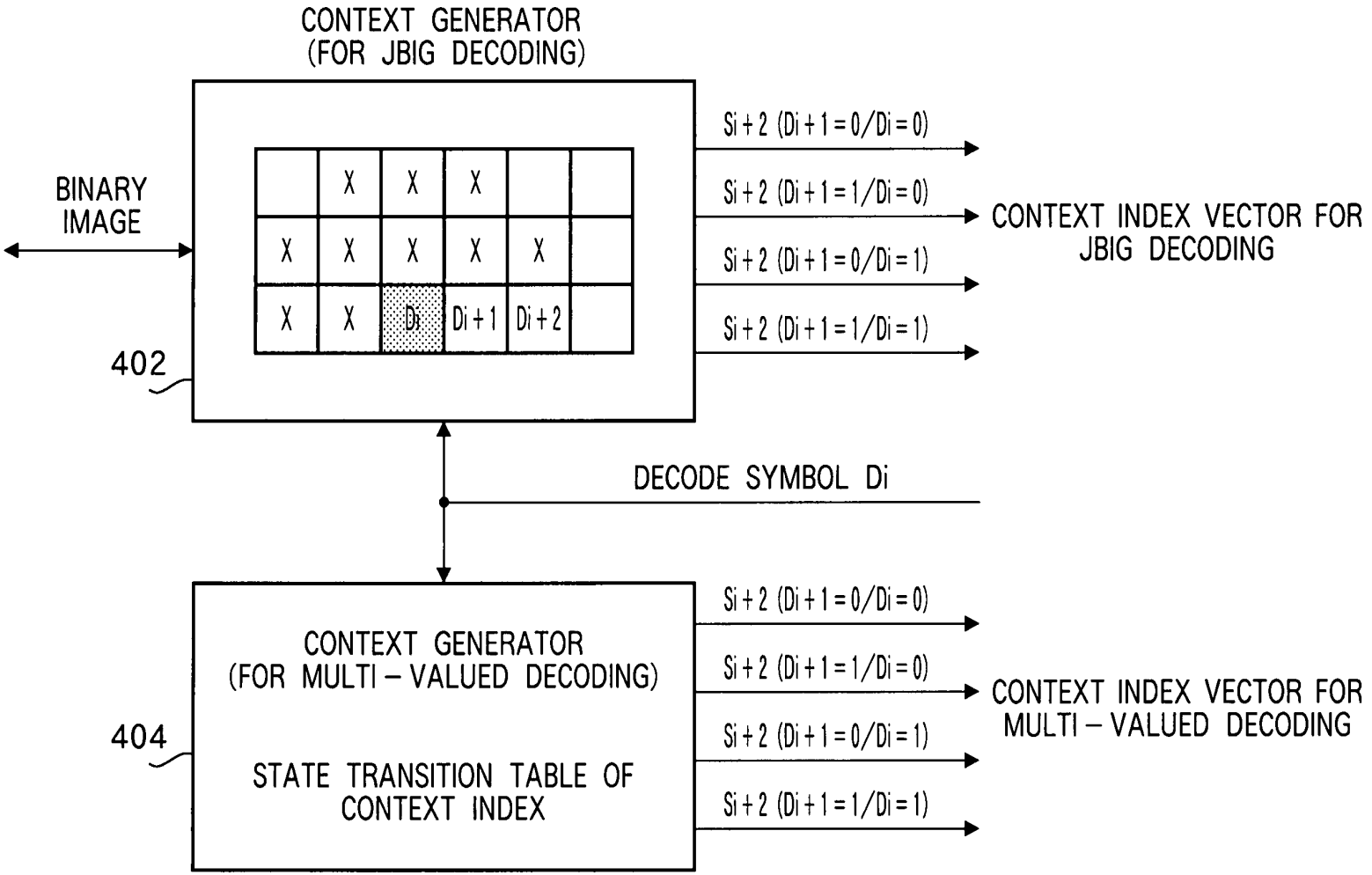

CONTEXT GENERATOR
(FOR JBIG DECODING)
BINARY
IMAGE
X
X
X
X
X
X
X
X
X
X
Di
Di+1
Di+2
402
Si+2 (Di+1=0/Di=0)
Si+2 (Di+1=1/Di=0)
Si+2 (Di+1=0/Di=1)
Si+2 (Di+1=1/Di=1)
CONTEXT INDEX VECTOR FOR
JBIG DECODING
DECODE SYMBOL Di
CONTEXT GENERATOR
(FOR MULTI-VALUED DECODING)
404
STATE TRANSITION TABLE OF
CONTEXT INDEX
Si+2 (Di+1=0/Di=0)
Si+2 (Di+1=1/Di=0)
Si+2 (Di+1=0/Di=1)
Si+2 (Di+1=1/Di=1)
CONTEXT INDEX VECTOR FOR
MULTI-VALUED DECODING

FIG.27

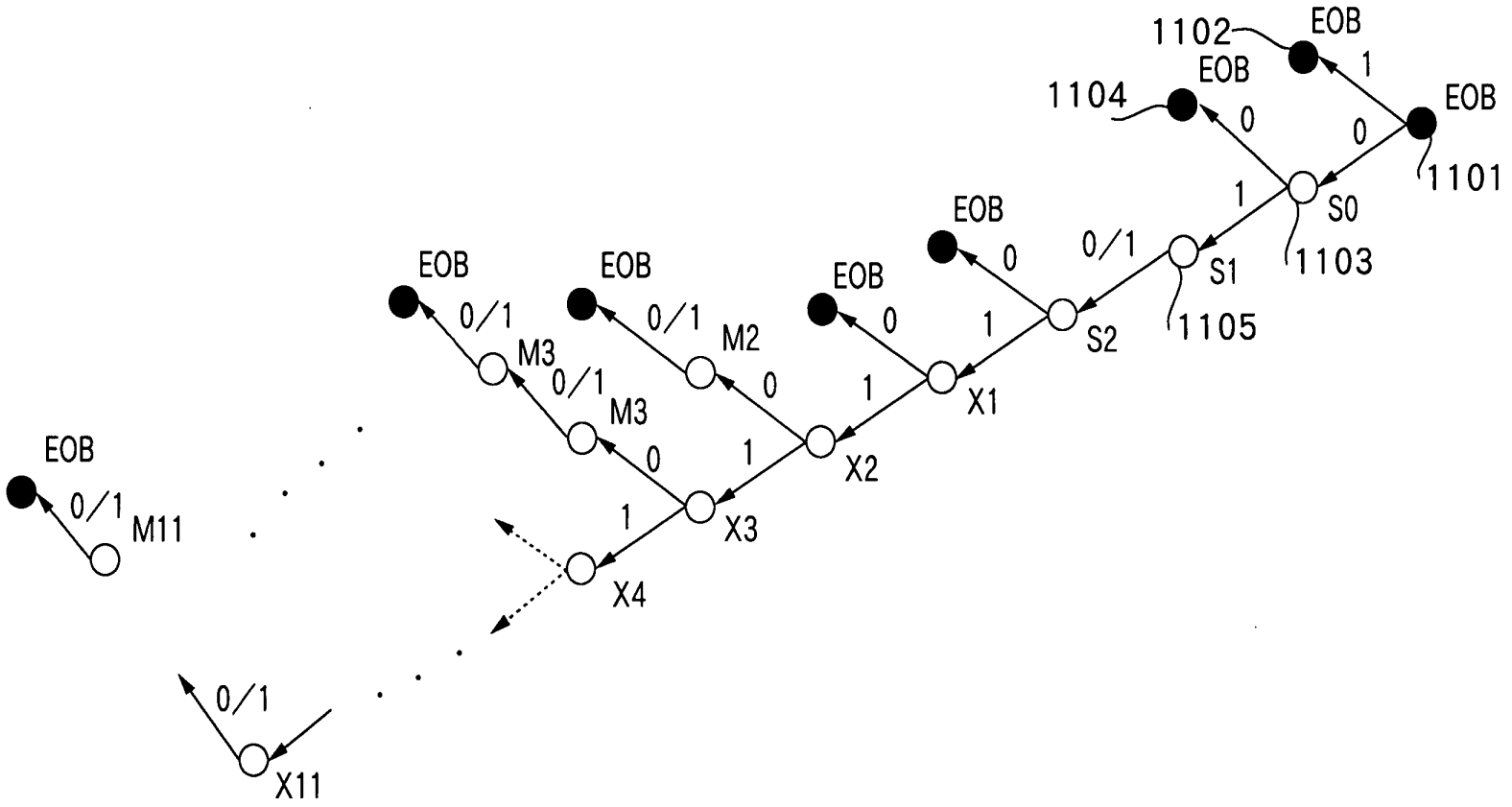

1102
EOB
1
EOB
1104
EOB
0
0
EOB
1101
1
S0
EOB
0
0/1
S1
1103
EOB
EOB
EOB
0/1
0/1
0
1
S2
1105
M3
M2
0/1
0
1
X1
M3
EOB
0
1
X2
0/1
M11
1
X3
X4
0/1
X11

FIG.28

STATE TRANSITION TABLE OF CONTEXT – INDEX (FOR DECODING)

1601 1602 1603 1604

STATE No.	Context(Si)		STATE (OUTPUT INDEX)				NEXT STATE	
			Di = 0		Di = 1			
	NAME	INDEX	Di + 1 = 0	Di + 1 = 1	Di + 1 = 0	Di + 1 = 1	Di = 0	Di = 1
0	EOB	0	0 (0)	2 (2)	1 (1)	0 (0)	1	0
1	S0	1	1 (1)	0 (0)	3 (3)	3 (3)	0	2
2	S1	2	0 (0)	4 (4)	0 (0)	4 (4)	3	3
3	S2	3	1 (1)	0 (0)	0 (0)	5 (5)	0	4
4	X1	4	1 (1)	0 (0)	15 (15)	6 (6)	0	5
5	X2	5	0 (0)	0 (0)	16 (16)	7 (7)	15	6
6	X3	6	17 (16)	18 (17)	19 (17)	8 (8)	16	7
7	X4	7	19 (17)	19 (17)	21 (18)	9 (9)	18	8
8	X5	8	22 (19)	22 (18)	25 (19)	10 (10)	21	9
9	X6	9	26 (19)	26 (19)	30 (20)	11 (11)	25	10
10	X7	10	31 (20)	31 (20)	36 (21)	12 (12)	30	11
11	X8	11	37 (21)	37 (21)	43 (22)	13 (13)	36	12
12	X9	12	44 (22)	44 (22)	51 (23)	14 (14)	43	13
13	X10	13	52 (23)	52 (23)	60 (24)	not def	51	14
14	X11	14	61 (24)	61 (24)	not def	not def	60	not def
15	M2	15	1 (1)	0 (0)	1 (1)	0 (0)	0	0
16	M3	16	0 (0)	0 (0)	0 (0)	0 (0)	17	17
17	M3	16	1 (1)	0 (0)	1 (1)	0 (0)	0	0
18	M4	17	20 (17)	20 (17)	20 (17)	20 (17)	19	19
19	M4	17	0 (0)	0 (0)	0 (0)	0 (0)	20	20
20	M4	17	1 (1)	0 (0)	1 (1)	0 (0)	0	0
21	M5	18	23 (18)	23 (18)	23 (18)	23 (18)	22	22
22	M5	18	24 (18)	24 (18)	24 (18)	24 (18)	23	23
23	M5	18	0 (0)	0 (0)	0 (0)	0 (0)	24	24
24	M5	18	1 (1)	0 (0)	1 (1)	0 (0)	0	0
25	M6	19	27 (19)	27 (19)	27 (19)	27 (19)	26	26
26	M6	19	28 (19)	28 (19)	28 (19)	28 (19)	27	27
27	M6	19	29 (19)	29 (19)	29 (19)	29 (19)	28	28
28	M6	19	0 (0)	0 (0)	0 (0)	0 (0)	29	29
29	M6	19	1 (1)	0 (0)	1 (1)	0 (0)	0	0
30	M7	20	32 (20)	32 (20)	32 (20)	32 (20)	31	31
31	M7	20	33 (20)	33 (20)	33 (20)	33 (20)	32	32
32	M7	20	34 (20)	34 (20)	34 (20)	34 (20)	33	33
33	M7	20	35 (20)	35 (20)	35 (20)	35 (20)	34	34
34	M7	20	0 (0)	0 (0)	0 (0)	0 (0)	35	35
35	M7	20	1 (1)	0 (0)	1 (1)	0 (0)	0	0
36	M8	21	38 (21)	38 (21)	38 (21)	38 (21)	37	37
37	M8	21	39 (21)	39 (21)	39 (21)	39 (21)	38	38
38	M8	21	40 (21)	40 (21)	40 (21)	40 (21)	39	39
39	M8	21	41 (21)	41 (21)	41 (21)	41 (21)	40	40
40	M8	21	42 (21)	42 (21)	42 (21)	42 (21)	41	41
41	M8	21	0 (0)	0 (0)	0 (0)	0 (0)	42	42
42	M8	21	0 (1)	0 (0)	1 (0)	0 (0)	0	0
43	M9	22	45 (22)	45 (22)	45 (22)	45 (22)	44	44
44	M9	22	46 (22)	46 (22)	46 (22)	46 (22)	45	45

FIG.29